PATENT ABSTRACTS OF JAPAN

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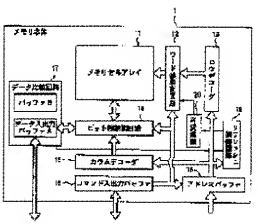
(54) NONVOLATILE SEMICONDUCTOR MEMORY

(57)Abstract:
PURPOSE: To obtain an EEPROM in which error due to the inversion of data is prevented.
CONSTITUTION: When an EEPROM is rewritten repeatedly, the gate oxide deteriorates gradually. But the extent of deterioration is low during the intermediate process and the original state of gate oxide can be thereby recovered. Data is then read out by applying different voltages to the memory cells in a memory cell array and it is decided whether the data being read out at a data comparison circuit 17 has same value thus detecting a variation in the threshold voltage of memory cell transistor. When a variation is detected in the threshold voltage, a data is rewritten. With such arrangement, transition in the state of held data can be prevented.



CLAIMS

[Claim(s)]
[Claim 1]A nonvolatile semiconductor memory comprising:
An information storage part which has one or two or more storage areas which consist of a nonvolatile memory cell transistor group in which a rewrite of data is possible.
A voltage source which generates voltage of a plural level for being impressed by a gate of said memory cell transistor.
A reading means which reads data from a memory cell transistor group of a storage area specified using voltage of the 1st level, or voltage of the 2nd level.
The 1st data retaining means holding data read using voltage of said 1st level, The 2nd data retaining means holding data read using voltage of said 2nd level, and a data comparison means which compares the data held at said 1st and 2nd data retaining means, and orders it a rewrite of data of said specified storage area based on a comparison result.

[Claim 2]A nonvolatile semiconductor memory comprising:
An information storage part which has one or two or more storage areas which consist of a nonvolatile memory cell transistor group in which a rewrite of data is possible.
A voltage source which generates voltage of a plural level for being impressed by a gate of said memory cell transistor.
A reading means which reads data from a memory cell transistor group of a storage area specified using voltage of the 1st level, voltage of the 2nd level, and voltage of a predetermined level.
The 1st data retaining means holding data read using voltage of said 1st level, The 2nd data retaining means holding data read using voltage of said 2nd level, The 3rd data retaining means holding data read using voltage of a predetermined level, A data comparison means which compares the data held at said 1st and 2nd data retaining means, and orders it a rewrite of data of said specified storage area based on a comparison result, A rewrite means by which data which answered instructions of said rewrite and was held at said 3rd data retaining means performs a rewrite of data of said specified storage area.

[Claim 3]A nonvolatile semiconductor memory comprising:
An information storage part which has one or two or more storage areas which consist of a nonvolatile memory cell transistor group in which a rewrite of data is possible.
A voltage source which generates voltage of a plural level for being impressed by a gate of said memory cell transistor.
A reading means which can read data from a memory cell transistor group of a storage area specified using voltage of the 1st level, voltage of the 2nd level, and voltage of a predetermined level.
The 1st data retaining means holding data read using voltage of said 1st level, The 2nd data retaining means holding data read using voltage of said 2nd level, A data comparison means which

compares the data held at said 1st and 2nd data retaining means, and orders it a rewrite of data of said specified storage area based on a comparison result, A rewrite means by which data which answered instructions of said rewrite, made data read from said specified storage area with voltage of said predetermined level, made hold this to said 1st [the] or said 2nd data retaining means, and was held performs a rewrite of data of said specified storage area.

[Claim 4]It is the method of distinguishing change of threshold voltage of a memory cell transistor in a nonvolatile semiconductor memory provided with two or more memory cell transistors which have a floating gate where it corresponds to data which should be held, and an electric charge is poured in or emitted in which a rewrite is possible, Voltage impressed to a gate of a memory cell transistor between usual threshold voltage of two memory cell transistors of a memory cell transistor to which a memory cell transistor and an electric charge into which an electric charge was poured were emitted is changed gradually, How to read data in voltage of each stage and distinguish change of threshold voltage of a memory cell transistor which distinguishes change of threshold voltage of a memory cell transistor by disagreement between data read on different voltage.
[Claim 5]The nonvolatile semiconductor memory according to any one of claims 1 to 3 characterized by what said voltage source generates voltage of a plural level objectively arranged on the basis of 0 volt and 0 volt for Masakata and in a negative direction for.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]Especially this invention relates to the nonvolatile semiconductor memory which improved the reliability of the data held by having a refresh function of stored data, concerning improvement of a rewritable nonvolatile semiconductor memory electrically.
[0002]
[Description of the Prior Art]NAND type EEPROM (Electrically Erasable PROM) in which high integration as shown in drawing 8 and drawing 9 is possible is electrically known as a rewritable nonvolatile semiconductor memory device, for example. Drawing 8 (a) shows the pattern of the memory cell for the single tier of EEPROM.
Drawing 8 (b) shows the electric equivalent circuit.
As for a control gate line and BL, in the figure, SG1 and SG2 are [the transistor for selection, M1 - M16] memory cells a bit line, S1, and S2 a selection line, CG1 - CG16. Drawing 9 (a) and drawing 9 (b) show roughly the sectional view of the semiconductor device which met in the direction of A-A'a direction and B-B' shown in drawing 8 (a), respectively. In both figures, 211 a semiconductor substrate and 212 the insulator layer of isolation, and 213 The insulator layer of a channel section (tunnel oxide film), 214 -- a floating gate and a forming [as for 215, / a control gate and 217 form an insulator layer, 218 forms a metal bit line (BL), and / 219]-gate insulation mesenteriolum and 216,-source drain area high concentration impurity region -- it comes out. As shown in drawing 8 and drawing 9, as NAND type EEPROM shares those sauce and the drain 219 between adjoining things, it connects mutually two or more memory cells M1 - M16 in series, makes this one unit and connects it to the bit line BL.
[0003]Each memory cell M usually has the FETMOS structure where the charge storage layer and the control gate 216 were laminated. the P type with which the memory cell array was formed in the substrate 211 of P type or N type -- a well -- accumulation formation is carried out inside. The drain side of a NAND cell is connected to a bit line via a selector gate, and the sauce side is too connected to a source line (reference potential wiring) via a selector gate. It is continuously connected to a line writing direction, and the control gate of a memory cell serves as a word line. Such a two or more rows memory cell sequence is established, and the actual memory cell array of EEPROM as shown in drawing 10 is formed.
[0004]Next, operation of NAND type EEPROM is explained. Writing and read-out of data are performed for every memory cell which shares a word line (CGi), as shown in drawing 10. This unit is called the page. Elimination of data is performed for every memory cell transistor which shares all the word lines (for example, CGi01 - CGi16) between two selector gates (for example, SGi1, SGi2), a drain side and the sauce side. This unit is called a block.
[0005]The writing of data impresses about [20V] high tension to the control gate of the selected memory cell transistor, and impresses about [10V] intermediate voltage to the control gate of the

non selection memory cell transistor of selected blocks, and the drain side selector gate of selected blocks. It is carried out by impressing 0V to the sauce side selector gate of selected blocks, and the selector gate of a non selection block, and impressing 0V or about [8V] intermediate voltage to the bit line BL according to write data, respectively. The voltage impressed to the bit line BL is transmitted to the channel of the selected memory cell transistor, when 0V is impressed, electron injection arises from a channel in a floating gate, and the threshold voltage of the selected memory cell transistor is shifted for Masakata. When 8V is impressed, electron injection does not happen, and the threshold voltage of a memory cell transistor does not change.

[0006]elimination of data -- a control gate -- 0V -- a P type board or an N type board, and P type -- it is carried out by impressing about [20V] high tension to a well, all the selector gates, and all the control gates of a non selection block, respectively. the incorrect writing generally according to the intermediate voltage at the time of writing -- it is rare (if only a certain page is written in and elimination is repeated, other pages within the block should be incorrect-written in) -- in order to prevent, it eliminates by a block unit, but elimination in a page unit is also technically possible. A bit line and a source line are made into floating. The electrons of a floating gate are emitted to a channel by all the memory cell transistors of the selected block by this, and threshold voltage is shifted to a negative direction. On the other hand, change of the threshold voltage of the memory cell transistor of a non selection block is not produced.

[0007]Read-out impresses 0V to the control gate of the memory cell transistor of the selected word line. Power supply voltage is impressed to the control gate and selector gate of a memory cell transistor of the other word line, respectively, and they are made to flow through all transistors other than the selected memory cell transistor. Read-out of data is performed by detecting whether current flows by the selected memory cell transistor.

[0008]

[Problem(s) to be Solved by the Invention]The data storage in the memory cell of EEPROM is making "0" and "1" memorize by whether an electron exists all over a floating gate, as mentioned above. Pouring/discharge of the electron to a floating gate are performed by sending current in a substrate and the oxide film between floating gates.

[0009]Therefore, if writing/erasing operation is repeated to EEPROM and performed to it, the characteristic of an oxide film deteriorates and it is known that the data holding characteristics of a memory cell will get worse gradually.

[0010]Although the grade of degradation of data holding characteristics is not fixed by the variation in the result of a cell, especially about the cell of the result, what cannot satisfy ten years which are a general lifetime guarantee period of a device occurs especially.

[0011]In the conventional unvolatilized student semiconductor memory device, if the bad cell of holding property occurs and data is reversed by data-hold error, the reversed data is unrestorable within a device. In this case, out of a device, an error restoration (ECC) circuit must be provided and it must be coped with.

[0012]In providing an error recovery circuit and restoring error data, Like NANDEEPROM (for example, TC5816 FT/TR (product name)) of 16 M bit capacity, In order that the data volume (data volume of 1 page) exchanged at once might enable error restoration to what is 256 bytes, the redundant bit had to be added, the data volume of 1 page had to be 264 bytes, and it had to let the error recovery circuit pass.

[0013]Therefore, even if the data holding characteristics of a memory cell deteriorate, this invention performs the rewrite of the held data of a memory cell to the inside of a state restorable within memory storage, and an object of this invention is to prevent the error by reversal of data beforehand and to improve the reliability of an unvolatilized student semiconductor memory device.

[0014]

[Means for Solving the Problem]In order to attain the above-mentioned purpose, an unvolatilized student semiconductor memory device of this invention. An information storage part which has one

or two or more storage areas which consist of a nonvolatile memory cell transistor group in which a rewrite of data is possible, A voltage source which generates voltage of a plural level for being impressed by a gate of the above-mentioned memory cell transistor, A reading means which reads data from a memory cell transistor group of a storage area specified using voltage of the 1st level, or voltage of the 2nd level, The 1st data retaining means holding data read using voltage of the 1st level of the above, It has the 2nd data retaining means holding data read using voltage of the 2nd level of the above, and a data comparison means which compares the data held at the 1st and 2nd data retaining means of the above, and orders it a rewrite of data of said specified storage area based on a comparison result.

[0015]A method of distinguishing change of threshold voltage of a memory cell transistor of this invention, In a method of distinguishing change of threshold voltage of a memory cell transistor in a nonvolatile semiconductor memory provided with two or more memory cell transistors which have a floating gate where it corresponds to data which should be held, and an electric charge is poured in or emitted in which a rewrite is possible, Voltage impressed to a gate of a memory cell transistor between usual threshold voltage of two memory cell transistors of a memory cell transistor to which a memory cell transistor and an electric charge into which an electric charge was poured were emitted is changed gradually, Change of threshold voltage of a memory cell transistor is distinguished by disagreement between data which read data in voltage of each stage and was read on different voltage.

[0016]

[Function]The data holding characteristics of the memory cell deteriorate gradually, if EEPROM is repeated and rewritten. However, in the process in the middle of deteriorating, since the grade of degradation is small, it is restorable in the original state.

[0017]Then, gate voltage which is different in a memory cell is impressed, data is read, it distinguishes whether the value of the data read is the same, and change of threshold voltage is detected. When threshold voltage is changing, the change state of held data is prevented by performing the rewrite of data.

[0018]

[Example]First, before describing the example of this invention, change of the threshold in NAND type EEPROM is explained. In the state of the electroneutrality the electron hole (hole) in the floating gate of a memory cell and whose number of electronic (electron) corresponded, it is designed and the threshold voltage of the cell is manufactured so that it may become near abbreviated 0 volt.

[0019]Where an electron is poured in into a floating gate (writing operation), threshold voltage turns into positive voltage, and where electrons are emitted (erasing state), threshold voltage turns into negative voltage from a floating gate. When it is neglected as it is, the cell group used as the cell group used as positive threshold voltage or negative threshold voltage is the other side to a neutral state electrically, as shown in drawing 2. Each cell is that over there electrically through a long time at a neutral state, and there is no trouble in use of a memory.

[0020]However, if writing/erasing operation is repeated, as shown in drawing 2 as a and b, the cell from which threshold voltage changes for a short time may appear. This becomes poor [data-hold]. By impressing voltage to a control gate at the time of read-out, as shown in drawing 3 as c, negative threshold voltage may already exceed 0 volt of ** from the time of neglect, and the cell used as positive threshold voltage may occur. It becomes poor read-out blocking this (Read Disturb).

[0021]Drawing 4 (A) shows the gate voltage versus drain current characteristic of the memory cell. The cell group (electron emission) in which data "1" was written serves as a DEYUPURESSHON type transistor into which current flows with the gate voltage of 0 volt. The cell group (electron emission) in which data "0" was written serves as a transistor into which current flows with the gate voltage of 0.5 volts or more, for example. In the cell with poor data-hold mentioned above, as

shown in drawing 4 (B) or the figure (C), it becomes the characteristic which the gate voltage versus drain current characteristic shifted.

[0022]Drawing 1 shows the example of this invention.

The memory cell array which, as for the semiconductor nonvolatile memory 1, 11 becomes from NAND type EEPROM, The word line driving circuit which drives the word line with which 12 is specified, the row decoder which orders the word line driving circuit 2 the drive of the word line corresponding to the address signal to which 13 was given, The control circuit which drives the bit line with which 14 was directed, the column decoder which orders it the drive of the bit line corresponding to the address signal to which 15 is given, The address buffer with which 16 holds an address signal temporarily, and 17 are provided with the data buffers A and B which hold an I/O data temporarily, A data comparator circuit provided with the function which compares data festering in both data buffers, The command input output buffer where 18 saves the command given to a memory temporarily, the variable voltage source which impresses the refresh control circuit where 19 controls refreshment (rewrite) of a memory cell array, and 20 to the gate of each memory cell, for example, generates +0.5 volts, +0.1 volts, and two or more 0-volt gate voltage of -0.1 volt-0.5 volt -- it comes out.

[0023]Next, operation of semiconductor memory is explained. The data which should write the writing of data in the data input/output buffer A of 17 of a data comparator circuit from CPU of the exterior which is not illustrated is supplied. A write command is supplied to the command input output buffer 18 from CPU, and a write-in address is supplied to the address buffer 16, respectively. As a result, the writing of data is performed to the memory cell array corresponding to the appointed address in the memory cell array 1.

[0024]Elimination of data is performed by supplying a deletion command to the command input output buffer 18 from CPU, and supplying an address signal to the address buffer 6, and carries out an address, and the data of the applicable memory cell in the memory cell array 1 which acted as Tay is cleared.

[0025]It reads from CPU, a command is supplied to the command input output buffer 18, and read-out of data is performed by giving a read address to the address buffer 16. Memory cell array 1 The data read from the applicable memory cell in one is outputted outside through the bit line control circuit 14 and the data input/output buffer A, and is incorporated into CPU which is not illustrated.

[0026]Next, error prevention of the held data based on lead stress is explained with reference to the flow chart shown in drawing 5.

[0027]NAND type EEPROM is controlled to write in the threshold voltage of the cell corresponding to data "0", and to sometimes become more than arbitrary voltage (for example, +0.5V). It is controlled so that similarly the threshold voltage of the cell corresponding to data "1" also turns into below arbitrary voltage (for example, -0.5V). The threshold voltage of what is called a neutral state with which the number of the electron all over a floating gate and electron holes balanced is in the 0V neighborhood.

[0028]then -- this example -- in the other case, the other case and the cell of "0" separate the data-hold error of a cell from +0.5V from -0.5V 0V 0V, and the cell of "1" verifies read-out data.

[0029]First, the refresh control circuit 19 starts execution of the control procedure shown in drawing 5 ignited by supply of the real line command of the data rewrite routine from CPU of the exterior which is not illustrated ignited by supply of the power turn reset signal to the storage device 1 which is not illustrated. The refresh control circuit 19 resets the rewriting flag F (S12). The page P which reads data from the memory cell array 11 is set to 1, and a read-out page address is set up via the row decoder 13 and the column decoder 15 (S14). The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as +0.5 volts, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses +0.5 volts to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The data for 1 page read from each page

[1st] memory cell is stored in the data input/output buffer (register) A of the data comparator circuit 17 through the bit line drive circuit 14 (S16).

[0030]Subsequently, the refresh control circuit 19 sets the output voltage of the variable voltage source 20 as +0.1 volts, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses +0.1 volts to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer (register) B of the data comparator circuit 17 through the bit line drive circuit 14 (S18).

[0031]It is distinguished whether the data stored in the data input/output buffers A and B is in agreement (S20). By comparing the data stored in the data input/output buffers A and B, as shown in drawing 4 (B), the cell which the threshold voltage of the memory cell shifted from +0.5 volt in the direction of 0 volt is detectable. In this case, the shift of threshold voltage appears as that from which "0" data changes to "0" from "1." When disagreement arises to the gate voltage of +0.5 volts, and +0.1-volt read-out data, the rewriting flag F which shows what a rewrite should be behind performed for is set to "1" (S22).

[0032]After setting the rewriting flag F when coincidence of data is distinguished (S20) or (S22), the refresh control circuit 19 sets the output voltage of the variable voltage source 20 as -0.5 volt, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses -0.5 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer A of the data comparator circuit 17 through the bit line drive circuit 14 (S24).

[0033]The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as -0.1 volt, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses -0.1 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer B of the data comparator circuit 17 through the bit line drive circuit 14 (S26).

[0034]It is distinguished whether the data stored in the data input/output buffers A and B is in agreement (S28). By comparing the data stored in the data input/output buffers A and B, as shown in drawing 4 (C), the cell which the threshold voltage of the memory cell shifted from -0.5 volt in the direction of 0 volt is detectable. In this case, the shift of threshold voltage appears as that from which "1" data changes to "1" from "0." When disagreement arises to read-out data (gate voltage-0.5 volt and -0.1 volt), the rewriting flag F is set to "1" (S30).

[0035]If the rewriting flag F is set (S32), all the page [1st] data is read from the memory cell array 10 with the usual gate bias voltage of 0 volt, and it stores in the data input/output buffer A. All the page [1st] data is eliminated and the page [1st] data stored in the data input/output buffer A is again written in the 1st page of the memory cell array 10. The threshold of each page [1st] memory cell is set as a reference value by this rewrite. The threshold voltage of the memory cell in which the absolute value decreased is corrected (S34).

[0036]A checked object page is set as the next page, and the rewriting flag F is reset (S36). To the page of the last of the memory cell array 10, Steps S16-S36 are repeated, the data of the page containing the memory cell which change produced in threshold voltage is rewritten, and generating of an error is prevented beforehand.

[0037]After distinction of the last page and a rewrite are completed, it returns to the original state of memory storage, or the original routine (S38).

[0038]In the above-mentioned example, it compares using the data input/output buffers A and B, and the rewrite data read after comparison is considered as the composition held to input-output-buffer A. It is possible to form the 3rd buffer, if there is a circuit space, and for rewrite data to be held to the 3rd buffer, and for it to be made to perform a rewrite with this data. In this case, it may be made to, hold the data read to the 3rd buffer at 0 volt as data for rewrting for example, following Steps S16 and S18. Also in the below-mentioned step S56, it is the same.

[0039]Drawing 6 shows the 2nd example.
Identical codes are given to the example shown in drawing 5, and a corresponding portion, and explanation of this portion is omitted.

[0040]In the figure, the refresh control circuit 19 resets a rewriting flag (S12), and sets an object page as the 1st page (S14). The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as +0.5 volts, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses +0.5 volts to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI, and reads page [1st] data. The data for 1 page read from each page [1st] memory cell is stored in the data input/output buffer (register) A of the data comparator circuit 17 through the bit line drive circuit 14 (S16).
[0041]Subsequently, the refresh control circuit 19 sets the output voltage of the variable voltage source 20 as +0.1 volts, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses +0.1 volts to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer (register) B of the data comparator circuit 17 through the bit line drive circuit 14.
[0042]It is distinguished whether the data stored in the data input/output buffers A and B is in agreement (S42). By comparing the data stored in the data input/output buffers A and B, as shown in drawing 4 (B), the cell which the threshold voltage of the memory cell shifted from +0.5 volt in the direction of 0 volt is detectable. In this case, the shift of threshold voltage appears as that from which "0" data changes to "0" from "1." When disagreement arises to the gate voltage of +0.5 volts, and +0.1-volt read-out data, the rewriting flag F which shows what a rewrite should be behind performed for is set to "1" (S44).
[0043]Next, the refresh control circuit 19 sets the output voltage of the variable voltage source 20 as -0.5 volt, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses -0.5 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer B of the data comparator circuit 17 through the bit line drive circuit 14.
[0044]It is distinguished whether the data which was stored in the data input/output buffers A and B and which was read at +0.5 volts and the data read by -0.5 volt are in agreement (S46). By comparing the data stored in the data input/output buffers A and B, as shown in drawing 4 (A), change of the threshold voltage of the memory cell in +0.5 volts which is a design identifiable range - -0.5 volt is detectable. When disagreement arises to the gate voltage of +0.5 volts, and -0.5 volt read-out data, the rewriting flag F which shows what a rewrite should be behind performed for is set to "1" (S48).
[0045]The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as -0.1 volt, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses -0.1 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer B of the data comparator circuit 17 through the bit line drive circuit 14.
[0046]It is distinguished whether the data which was stored in the data input/output buffers A and B and which was read at +0.5 volts and the data read by -0.1 volt are in agreement (S50). By comparing the data stored in the data input/output buffers A and B, change of the threshold voltage of the memory cell in +0.5 volts - -0.1 volt is detectable. When disagreement arises to the gate voltage of +0.5 volts, and -0.1 volt read-out data, the rewriting flag F which shows what a rewrite should be behind performed for is set to "1" (S52).
[0047]If the rewriting flag F is set to "1" (S32), all the page [1st] data is read from the memory cell array 10 with the usual gate bias voltage of 0 volt, and it stores in the data input/output buffer A. All the page [1st] data of the memory cell array 10 is eliminated, and the page [1st] data

stored in the data input/output buffer A is again written in the 1st page of the memory cell array 10. The threshold of each page [1st] memory cell is set as a reference value by this rewrite. The threshold voltage of the memory cell in which the absolute value decreased is corrected (S56).

[0048]Hereafter, set a checked object page as the next page, reset the rewriting flag F like drawing 5 (S36), and to the page of the last of the memory cell array 10, Steps S16-S36 are repeated, the data of the page containing the memory cell which change produced in threshold voltage is rewritten, and generating of an error is prevented beforehand.

[0049]After distinction of the last page and a rewrite are completed, it returns to the original state of memory storage, or the original routine (S38).

[0050]The 3rd example is shown in drawing 7. In the figure, identical codes are given to drawing 5 and a corresponding step. In this example, the value change is seen on the basis of the data read at 0 volt. Access from CPU is taken into consideration and distinction of the existence of an error is enabled every page of each 11 of the memory cell array.

[0051]First, the refresh control circuit 19 resets error flag F1 - Fn which were set as the specific memory location of a memory cell array and which were prepared by n page corresponding to each page (S12), and sets the page P of a checked object as 1 page (S14).

[0052]The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as 0 volt which is standard gate impressed electromotive force, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses 0 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The data for 1 page read from each page [1st] memory cell is stored in the data input/output buffer A of the data comparator circuit 17 through the bit line drive circuit 14 (S62).

[0053]Next, a +0.5-volt read-out check is performed. The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as +0.5 volts, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses +0.5 volts to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The data for 1 page read from each page [1st] memory cell is stored in the data input/output buffer B of the data comparator circuit 17 through the bit line drive circuit 14. In the data comparator circuit 17, the value of the data input/output buffers A and B is compared, and it is confirmed whether the read-out data based on regular gate voltage (0 volt) and the read-out data based on +0.5 volts are in agreement (S64). Since the shift of the threshold voltage of data "0" can be considered within the limits of 0-+0.5 volts when not in agreement, the error flag Fp (at the time of the page 1, it is F1) formed for every page is set as "1" (S66).

[0054]-Perform a 0.5-volt check. The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as -0.5 volt, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses -0.5 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The data for 1 page read from each page [1st] memory cell is stored in the data input/output buffer B of the data comparator circuit 17 through the bit line drive circuit 14. In the data comparator circuit 17, the value of the data input/output buffers A and B is compared, and it is confirmed whether the read-out data based on regular gate voltage (0 volt) and the read-out data based on -0.5 volt are in agreement (S68). Since the shift of the threshold voltage of data "1" can be considered within the limits of 0--0.5 volt when not in agreement, the error flag Fp is set as "1" (S70).

[0055]The page for error checking is set as the following page (S36), Steps S62-S70 are repeated, and error checking is performed to the last page (S38). The checked result of each page can be read by referring to a flag. Therefore, it is possible to make execution of this check routine direct from external CPU, to make the contents of the error flag read to CPU, and to make the rewrite of necessary data perform.

[0056]Also in this example, error checking can be performed like Step [which was mentioned above] S34 and S56 based on the result of error checking.

[0057]In each example mentioned above, error checking is performed about all the storage areas in

a memory. However, some storage areas may be checked and it may decide to rewrite all storage areas by the result. It is good also as distinguishing whether the start page (memory location) of a check is specified in Step S14 mentioned above, and it is in agreement with the page of the end of a check at Step S38. For example, an initial program loader (Initial Program Loader) and an operating system portion with read-out frequency high among the programs recorded on EEPROM can be considered as contrast of a check.

[0058]Although the updating (rewrite) unit of data explained the page as a unit in the example, it is not limited to this. For example, it is possible to perform as a unit the cluster which is the set of a block and a block which is a set of a page.

[0059]According to each example of this invention mentioned above, impress voltage which is different to the gate of a memory cell, and data is read. Since the threshold voltage corresponding to the data which the threshold voltage of each memory cell holds resets before it distinguishes the shift of threshold voltage and threshold voltage exceeds the distinction limit of "0" or "1" data according to a difference of the data read, reversal of the held data of EEPROM is prevented.

[0060]

[Effect of the Invention]In [as explained above] nonvolatile memory rewritable in this invention, Before the error arose by the change state of the held data based on threshold change of a memory cell transistor, when the data which changed the voltage impressed to the gate of a memory cell transistor near the reference value, and read it was compared and data had an error, it was made to perform the rewrite of data.

Therefore, it becomes possible without being influenced by the read number to continue holding right data.

Since it is necessary to provide neither the error correction circuit (ECC) of data complicated the exterior or inside memory storage, nor the redundant bit for making an error correction possible into a page, it is in good order.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application]Especially this invention relates to the nonvolatile semiconductor memory which improved the reliability of the data held by having a refresh function of stored data, concerning improvement of a rewritable nonvolatile semiconductor memory electrically.

[Translation done.]

PRIOR ART

[Description of the Prior Art]NAND type EEPROM (Electrically Erasable PROM) in which high integration as shown in drawing 8 and drawing 9 is possible is electrically known as a rewritable nonvolatile semiconductor memory device, for example. Drawing 8 (a) shows the pattern of the memory cell for the single tier of EEPROM.
Drawing 8 (b) shows the electric equivalent circuit.
As for a control gate line and BL, in the figure, SG1 and SG2 are [the transistor for selection, M1 - M16] memory cells a bit line, S1, and S2 a selection line, CG1 - CG16. Drawing 9 (a) and drawing 9 (b) show roughly the sectional view of the semiconductor device which met in the direction of A-A'a direction and B-B' shown in drawing 8 (a), respectively. In both figures, 211 a semiconductor substrate and 212 the insulator layer of isolation, and 213 The insulator layer of a channel section (tunnel oxide film), 214 -- a floating gate and a forming [as for 215, / a control gate and 217 form an insulator layer, 218 forms a metal bit line (BL), and / 219]-gate insulation mesenteriolum and 216,-source drain area high concentration impurity region -- it comes out. As shown in drawing 8 and drawing 9, as NAND type EEPROM shares those sauce and the drain 219 between adjoining things, it connects mutually two or more memory cells M1 - M16 in series, makes this one unit and connects it to the bit line BL.
[0003]Each memory cell M usually has the FETMOS structure where the charge storage layer and the control gate 216 were laminated. the P type with which the memory cell array was formed in the substrate 211 of P type or N type -- a well -- accumulation formation is carried out inside. The drain side of a NAND cell is connected to a bit line via a selector gate, and the sauce side is too connected to a source line (reference potential wiring) via a selector gate. It is continuously connected to a line writing direction, and the control gate of a memory cell serves as a word line. Such a two or more rows memory cell sequence is established, and the actual memory cell array of EEPROM as shown in drawing 10 is formed.
[0004]Next, operation of NAND type EEPROM is explained. Writing and read-out of data are performed for every memory cell which shares a word line (CGi), as shown in drawing 10. This unit is called the page. Elimination of data is performed for every memory cell transistor which shares all the word lines (for example, CGi01 - CGi16) between two selector gates (for example, SGi1, SGi2), a drain side and the sauce side. This unit is called a block.
[0005]The writing of data impresses about [20V] high tension to the control gate of the selected memory cell transistor, and impresses about [10V] intermediate voltage to the control gate of the non selection memory cell transistor of selected blocks, and the drain side selector gate of selected blocks. It is carried out by impressing 0V to the sauce side selector gate of selected blocks, and the selector gate of a non selection block, and impressing 0V or about [8V] intermediate voltage to the bit line BL according to write data, respectively. The voltage impressed to the bit line BL is transmitted to the channel of the selected memory cell transistor, when 0V is impressed, electron injection arises from a channel in a floating gate, and the threshold voltage of the selected memory

cell transistor is shifted for Masakata. When 8V is impressed, electron injection does not happen, and the threshold voltage of a memory cell transistor does not change.

[0006]elimination of data -- a control gate -- 0V -- a P type board or an N type board, and P type -- it is carried out by impressing about [20V] high tension to a well, all the selector gates, and all the control gates of a non selection block, respectively. the incorrect writing generally according to the intermediate voltage at the time of writing -- it is rare (if only a certain page is written in and elimination is repeated, other pages within the block should be incorrect-written in) -- in order to prevent, it eliminates by a block unit, but elimination in a page unit is also technically possible. A bit line and a source line are made into floating. The electrons of a floating gate are emitted to a channel by all the memory cell transistors of the selected block by this, and threshold voltage is shifted to a negative direction. On the other hand, change of the threshold voltage of the memory cell transistor of a non selection block is not produced.

[0007]Read-out impresses 0V to the control gate of the memory cell transistor of the selected word line. Power supply voltage is impressed to the control gate and selector gate of a memory cell transistor of the other word line, respectively, and they are made to flow through all transistors other than the selected memory cell transistor. Read-out of data is performed by detecting whether current flows by the selected memory cell transistor.

[Translation done.]

* NOTICES *

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EFFECT OF THE INVENTION

[Effect of the Invention]In [as explained above] nonvolatile memory rewritable in this invention, Before the error arose by the change state of the held data based on threshold change of a memory cell transistor, when the data which changed the voltage impressed to the gate of a memory cell transistor near the reference value, and read it was compared and data had an error, it was made to perform the rewrite of data.
Therefore, it becomes possible without being influenced by the read number to continue holding right data.
Since it is necessary to provide neither the error correction circuit (ECC) of data complicated the exterior or inside memory storage, nor the redundant bit for making an error correction possible into a page, it is in good order.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]The data storage in the memory cell of EEPROM is making "0" and "1" memorize by whether an electron exists all over a floating gate, as mentioned above. Pouring/discharge of the electron to a floating gate are performed by sending current in a substrate and the oxide film between floating gates.
[0009]Therefore, if writing/erasing operation is repeated to EEPROM and performed to it, the characteristic of an oxide film deteriorates and it is known that the data holding characteristics of a memory cell will get worse gradually.
[0010]Although the grade of degradation of data holding characteristics is not fixed by the variation in the result of a cell, especially about the cell of the result, what cannot satisfy ten years which are a general lifetime guarantee period of a device occurs especially.
[0011]In the conventional unvolatilized student semiconductor memory device, if the bad cell of holding property occurs and data is reversed by data-hold error, the reversed data is unrestorable within a device. In this case, out of a device, an error restoration (ECC) circuit must be provided and it must be coped with.
[0012]In providing an error recovery circuit and restoring error data, Like NANDEEPROM (for example, TC5816 FT/TR (product name)) of 16 M bit capacity, In order that the data volume (data volume of 1 page) exchanged at once might enable error restoration to what is 256 bytes, the redundant bit had to be added, the data volume of 1 page had to be 264 bytes, and it had to let the error recovery circuit pass.
[0013]Therefore, even if the data holding characteristics of a memory cell deteriorate, this invention performs the rewrite of the held data of a memory cell to the inside of a state restorable within memory storage, and an object of this invention is to prevent the error by reversal of data beforehand and to improve the reliability of an unvolatilized student semiconductor memory device.

[Translation done.]

MEANS

[Means for Solving the Problem]In order to attain the above-mentioned purpose, an unvolatilized student semiconductor memory device of this invention, An information storage part which has one or two or more storage areas which consist of a nonvolatile memory cell transistor group in which a rewrite of data is possible, A voltage source which generates voltage of a plural level for being impressed by a gate of the above-mentioned memory cell transistor, A reading means which reads data from a memory cell transistor group of a storage area specified using voltage of the 1st level, or voltage of the 2nd level, The 1st data retaining means holding data read using voltage of the 1st level of the above, It has the 2nd data retaining means holding data read using voltage of the 2nd level of the above, and a data comparison means which compares the data held at the 1st and 2nd data retaining means of the above, and orders it a rewrite of data of said specified storage area based on a comparison result.
[0015]A method of distinguishing change of threshold voltage of a memory cell transistor of this invention, In a method of distinguishing change of threshold voltage of a memory cell transistor in a nonvolatile semiconductor memory provided with two or more memory cell transistors which have a floating gate where it corresponds to data which should be held, and an electric charge is poured in or emitted in which a rewrite is possible, Voltage impressed to a gate of a memory cell transistor between usual threshold voltage of two memory cell transistors of a memory cell transistor to which a memory cell transistor and an electric charge into which an electric charge was poured were emitted is changed gradually, Change of threshold voltage of a memory cell transistor is distinguished by disagreement between data which read data in voltage of each stage and was read on different voltage.

[Translation done.]

OPERATION

[Function]The data holding characteristics of the memory cell deteriorate gradually, if EEPROM is repeated and rewritten. However, in the process in the middle of deteriorating, since the grade of degradation is small, it is restorable in the original state.
[0017]Then, gate voltage which is different in a memory cell is impressed, data is read, it distinguishes whether the value of the data read is the same, and change of threshold voltage is detected. When threshold voltage is changing, the change state of held data is prevented by performing the rewrite of data.

[Translation done.]

EXAMPLE

[Example]First, before describing the example of this invention, change of the threshold in NAND type EEPROM is explained. In the state of the electroneutrality the electron hole (hole) in the floating gate of a memory cell and whose number of electronic (electron) corresponded, it is designed and the threshold voltage of the cell is manufactured so that it may become near abbreviated 0 volt.
[0019]Where an electron is poured in into a floating gate (writing operation), threshold voltage turns into positive voltage, and where electrons are emitted (erasing state), threshold voltage turns into negative voltage from a floating gate. When it is neglected as it is, the cell group used as the cell group used as positive threshold voltage or negative threshold voltage is the other side to a neutral state electrically, as shown in drawing 2. Each cell is that over there electrically through a long time at a neutral state, and there is no trouble in use of a memory.
[0020]However, if writing/erasing operation is repeated, as shown in drawing 2 as a and b, the cell from which threshold voltage changes for a short time may appear. This becomes poor [data-hold]. By impressing voltage to a control gate at the time of read-out, as shown in drawing 3 as c, negative threshold voltage may already exceed 0 volt of ** from the time of neglect, and the cell used as positive threshold voltage may occur. It becomes poor read-out blocking this (Read Disturb).
[0021]Drawing 4 (A) shows the gate voltage versus drain current characteristic of the memory cell. The cell group (electron emission) in which data "1" was written serves as a DEYUPURESSHON type transistor into which current flows with the gate voltage of 0 volt. The cell group (electron emission) in which data "0" was written serves as a transistor into which current flows with the gate voltage of 0.5 volts or more, for example. In the cell with poor data-hold mentioned above, as shown in drawing 4 (B) or the figure (C), it becomes the characteristic which the gate voltage versus drain current characteristic shifted.
[0022]Drawing 1 shows the example of this invention.
The memory cell array which, as for the semiconductor nonvolatile memory 1, 11 becomes from NAND type EEPROM, The word line driving circuit which drives the word line with which 12 is specified, the row decoder which orders the word line driving circuit 2 the drive of the word line corresponding to the address signal to which 13 was given, The control circuit which drives the bit line with which 14 was directed, the column decoder which orders it the drive of the bit line corresponding to the address signal to which 15 is given, The address buffer with which 16 holds an address signal temporarily, and 17 are provided with the data buffers A and B which hold an I/O data temporarily, A data comparator circuit provided with the function which compares data festering in both data buffers, The command input output buffer where 18 saves the command given to a memory temporarily, the variable voltage source which impresses the refresh control circuit where 19 controls refreshment (rewrite) of a memory cell array, and 20 to the gate of each memory cell, for example, generates +0.5 volts, +0.1 volts, and two or more 0-volt gate voltage of -0.1 volt-

0.5 volt -- it comes out.

[0023]Next, operation of semiconductor memory is explained. The data which should write the writing of data in the data input/output buffer A of 17 of a data comparator circuit from CPU of the exterior which is not illustrated is supplied. A write command is supplied to the command input output buffer 18 from CPU, and a write-in address is supplied to the address buffer 16, respectively. As a result, the writing of data is performed to the memory cell array corresponding to the appointed address in the memory cell array 1.
[0024]Elimination of data is performed by supplying a deletion command to the command input output buffer 18 from CPU, and supplying an address signal to the address buffer 6, and carries out an address, and the data of the applicable memory cell in the memory cell array 1 which acted as Tay is cleared.
[0025]It reads from CPU, a command is supplied to the command input output buffer 18, and read-out of data is performed by giving a read address to the address buffer 16. Memory cell array 1 The data read from the applicable memory cell in one is outputted outside through the bit line control circuit 14 and the data input/output buffer A, and is incorporated into CPU which is not illustrated.
[0026]Next, error prevention of the held data based on lead stress is explained with reference to the flow chart shown in drawing 5.
[0027]NAND type EEPROM is controlled to write in the threshold voltage of the cell corresponding to data "0", and to sometimes become more than arbitrary voltage (for example, +0.5V). It is controlled so that similarly the threshold voltage of the cell corresponding to data "1" also turns into below arbitrary voltage (for example, -0.5V). The threshold voltage of what is called a neutral state with which the number of the electron all over a floating gate and electron holes balanced is in the 0V neighborhood.
[0028]then -- this example -- in the other case, the other case and the cell of "0" separate the data-hold error of a cell from +0.5V from -0.5V 0V 0V, and the cell of "1" verifies read-out data.
[0029]First, the refresh control circuit 19 starts execution of the control procedure shown in drawing 5 ignited by supply of the real line command of the data rewrite routine from CPU of the exterior which is not illustrated ignited by supply of the power turn reset signal to the storage device 1 which is not illustrated. The refresh control circuit 19 resets the rewriting flag F (S12). The page P which reads data from the memory cell array 11 is set to 1, and a read-out page address is set up via the row decoder 13 and the column decoder 15 (S14). The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as +0.5 volts, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses +0.5 volts to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The data for 1 page read from each page [1st] memory cell is stored in the data input/output buffer (register) A of the data comparator circuit 17 through the bit line drive circuit 14 (S16).
[0030]Subsequently, the refresh control circuit 19 sets the output voltage of the variable voltage source 20 as +0.1 volts, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses +0.1 volts to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer (register) B of the data comparator circuit 17 through the bit line drive circuit 14 (S18).
[0031]It is distinguished whether the data stored in the data input/output buffers A and B is in agreement (S20). By comparing the data stored in the data input/output buffers A and B, as shown in drawing 4 (B), the cell which the threshold voltage of the memory cell shifted from +0.5 volt in the direction of 0 volt is detectable. In this case, the shift of threshold voltage appears as that from which "0" data changes to "0" from "1." When disagreement arises to the gate voltage of +0.5 volts, and +0.1-volt read-out data, the rewriting flag F which shows what a rewrite should be behind performed for is set to "1" (S22).

[0032]After setting the rewriting flag F when coincidence of data is distinguished (S20) or (S22), the refresh control circuit 19 sets the output voltage of the variable voltage source 20 as −0.5 volt, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses −0.5 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer A of the data comparator circuit 17 through the bit line drive circuit 14 (S24).
[0033]The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as −0.1 volt, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses −0.1 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer B of the data comparator circuit 17 through the bit line drive circuit 14 (S26).
[0034]It is distinguished whether the data stored in the data input/output buffers A and B is in agreement (S28). By comparing the data stored in the data input/output buffers A and B, as shown in drawing 4 (C), the cell which the threshold voltage of the memory cell shifted from −0.5 volt in the direction of 0 volt is detectable. In this case, the shift of threshold voltage appears as that from which "1" data changes to "1" from "0." When disagreement arises to read-out data (gate voltage-0.5 volt and −0.1 volt), the rewriting flag F is set to "1" (S30).
[0035]If the rewriting flag F is set (S32), all the page [1st] data is read from the memory cell array 10 with the usual gate bias voltage of 0 volt, and it stores in the data input/output buffer A. All the page [1st] data is eliminated and the page [1st] data stored in the data input/output buffer A is again written in the 1st page of the memory cell array 10. The threshold of each page [1st] memory cell is set as a reference value by this rewrite. The threshold voltage of the memory cell in which the absolute value decreased is corrected (S34).
[0036]A checked object page is set as the next page, and the rewriting flag F is reset (S36). To the page of the last of the memory cell array 10, Steps S16-S36 are repeated, the data of the page containing the memory cell which change produced in threshold voltage is rewritten, and generating of an error is prevented beforehand.
[0037]After distinction of the last page and a rewrite are completed, it returns to the original state of memory storage, or the original routine (S38).
[0038]In the above-mentioned example, it compares using the data input/output buffers A and B, and the rewrite data read after comparison is considered as the composition held to input-output-buffer A. It is possible to form the 3rd buffer, if there is a circuit space, and for rewrite data to be held to the 3rd buffer, and for it to be made to perform a rewrite with this data. In this case, it may be made to, hold the data read to the 3rd buffer at 0 volt as data for rewrting for example, following Steps S16 and S18. Also in the below-mentioned step S56, it is the same.
[0039]Drawing 6 shows the 2nd example.
Identical codes are given to the example shown in drawing 5, and a corresponding portion, and explanation of this portion is omitted.

[0040]In the figure, the refresh control circuit 19 resets a rewriting flag (S12), and sets an object page as the 1st page (S14). The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as +0.5 volts, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses +0.5 volts to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI, and reads page [1st] data. The data for 1 page read from each page [1st] memory cell is stored in the data input/output buffer (register) A of the data comparator circuit 17 through the bit line drive circuit 14 (S16).
[0041]Subsequently, the refresh control circuit 19 sets the output voltage of the variable voltage source 20 as +0.1 volts, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses +0.1 volts to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data

input/output buffer (register) B of the data comparator circuit 17 through the bit line drive circuit 14.

[0042]It is distinguished whether the data stored in the data input/output buffers A and B is in agreement (S42). By comparing the data stored in the data input/output buffers A and B, as shown in drawing 4 (B), the cell which the threshold voltage of the memory cell shifted from +0.5 volt in the direction of 0 volt is detectable. In this case, the shift of threshold voltage appears as that from which "0" data changes to "0" from "1." When disagreement arises to the gate voltage of +0.5 volts, and +0.1-volt read-out data, the rewriting flag F which shows what a rewrite should be behind performed for is set to "1" (S44).

[0043]Next, the refresh control circuit 19 sets the output voltage of the variable voltage source 20 as -0.5 volt, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses -0.5 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer B of the data comparator circuit 17 through the bit line drive circuit 14.

[0044]It is distinguished whether the data which was stored in the data input/output buffers A and B and which was read at +0.5 volts and the data read by -0.5 volt are in agreement (S46). By comparing the data stored in the data input/output buffers A and B, as shown in drawing 4 (A), change of the threshold voltage of the memory cell in +0.5 volts which is a design identifiable range - -0.5 volt is detectable. When disagreement arises to the gate voltage of +0.5 volts, and -0.5 volt read-out data, the rewriting flag F which shows what a rewrite should be behind performed for is set to "1" (S48).

[0045]The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as -0.1 volt, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses -0.1 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The 1-page data read from each page [1st] memory cell is stored in the data input/output buffer B of the data comparator circuit 17 through the bit line drive circuit 14.

[0046]It is distinguished whether the data which was stored in the data input/output buffers A and B and which was read at +0.5 volts and the data read by -0.1 volt are in agreement (S50). By comparing the data stored in the data input/output buffers A and B, change of the threshold voltage of the memory cell in +0.5 volts - -0.1 volt is detectable. When disagreement arises to the gate voltage of +0.5 volts, and -0.1 volt read-out data, the rewriting flag F which shows what a rewrite should be behind performed for is set to "1" (S52).

[0047]If the rewriting flag F is set to "1" (S32), all the page [1st] data is read from the memory cell array 10 with the usual gate bias voltage of 0 volt, and it stores in the data input/output buffer A. All the page [1st] data of the memory cell array 10 is eliminated, and the page [1st] data stored in the data input/output buffer A is again written in the 1st page of the memory cell array 10. The threshold of each page [1st] memory cell is set as a reference value by this rewrite. The threshold voltage of the memory cell in which the absolute value decreased is corrected (S56).

[0048]Hereafter, set a checked object page as the next page, reset the rewriting flag F like drawing 5 (S36), and to the page of the last of the memory cell array 10, Steps S16-S36 are repeated, the data of the page containing the memory cell which change produced in threshold voltage is rewritten, and generating of an error is prevented beforehand.

[0049]After distinction of the last page and a rewrite are completed, it returns to the original state of memory storage, or the original routine (S38).

[0050]The 3rd example is shown in drawing 7. In the figure, identical codes are given to drawing 5 and a corresponding step. In this example, the value change is seen on the basis of the data read at 0 volt. Access from CPU is taken into consideration and distinction of the existence of an error is enabled every page of each 11 of the memory cell array.

[0051]First, the refresh control circuit 19 resets error flag F1 - Fn which were set as the specific memory location of a memory cell array and which were prepared by n page corresponding to each

page (S12), and sets the page P of a checked object as 1 page (S14).
[0052]The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as 0 volt which is standard gate impressed electromotive force, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses 0 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The data for 1 page read from each page [1st] memory cell is stored in the data input/output buffer A of the data comparator circuit 17 through the bit line drive circuit 14 (S62).
[0053]Next, a +0.5-volt read-out check is performed. The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as +0.5 volts, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses +0.5 volts to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The data for 1 page read from each page [1st] memory cell is stored in the data input/output buffer B of the data comparator circuit 17 through the bit line drive circuit 14. In the data comparator circuit 17, the value of the data input/output buffers A and B is compared, and it is confirmed whether the read-out data based on regular gate voltage (0 volt) and the read-out data based on +0.5 volts are in agreement (S64). Since the shift of the threshold voltage of data "0" can be considered within the limits of 0-+0.5 volts when not in agreement, the error flag Fp (at the time of the page 1, it is F1) formed for every page is set as "1" (S66).
[0054]-Perform a 0.5-volt check. The refresh control circuit 19 sets the output voltage of the variable voltage source 20 as -0.5 volt, and supplies it to the word line driving circuit 12. The word line driving circuit 12 impresses -0.5 volt to the gate of a page [1st] memory cell via the word line equivalent to 1st **-JI. The data for 1 page read from each page [1st] memory cell is stored in the data input/output buffer B of the data comparator circuit 17 through the bit line drive circuit 14. In the data comparator circuit 17, the value of the data input/output buffers A and B is compared, and it is confirmed whether the read-out data based on regular gate voltage (0 volt) and the read-out data based on -0.5 volt are in agreement (S68). Since the shift of the threshold voltage of data "1" can be considered within the limits of 0—0.5 volt when not in agreement, the error flag Fp is set as "1" (S70).
[0055]The page for error checking is set as the following page (S36), Steps S62-S70 are repeated, and error checking is performed to the last page (S38). The checked result of each page can be read by referring to a flag. Therefore, it is possible to make execution of this check routine direct from external CPU, to make the contents of the error flag read to CPU, and to make the rewrite of necessary data perform.
[0056]Also in this example, error checking can be performed like Step [which was mentioned above] S34 and S56 based on the result of error checking.
[0057]In each example mentioned above, error checking is performed about all the storage areas in a memory. However, some storage areas may be checked and it may decide to rewrite all storage areas by the result. It is good also as distinguishing whether the start page (memory location) of a check is specified in Step S14 mentioned above, and it is in agreement with the page of the end of a check at Step S38. For example, an initial program loader (Initial Program Loader) and an operating system portion with read-out frequency high among the programs recorded on EEPROM can be considered as contrast of a check.
[0058]Although the updating (rewrite) unit of data explained the page as a unit in the example, it is not limited to this. For example, it is possible to perform as a unit the cluster which is the set of a block and a block which is a set of a page.
[0059]According to each example of this invention mentioned above, impress voltage which is different to the gate of a memory cell, and data is read, Since the threshold voltage corresponding to the data which the threshold voltage of each memory cell holds resets before it distinguishes the shift of threshold voltage and threshold voltage exceeds the distinction limit of "0" or "1" data according to a difference of the data read, reversal of the held data of EEPROM is prevented.

[Translation done.]

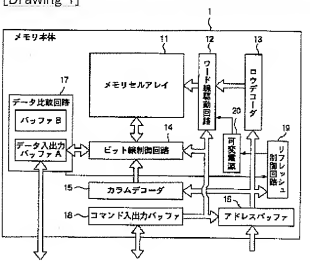
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block circuit diagram showing the example of this invention.
[Drawing 2]It is an explanatory view for explaining the change tendency of the threshold voltage of a memory cell transistor.
[Drawing 3]It is an explanatory view for explaining the error of the threshold in a memory cell transistor.
[Drawing 4]It is an explanatory view explaining the gate voltage versus drain current characteristic of a memory cell transistor group.
[Drawing 5]It is a flow chart explaining the rewriting operations of data.
[Drawing 6]It is a flow chart explaining the rewriting operations of data.
[Drawing 7]It is a flow chart explaining the operation which checks a threshold shift.
[Drawing 8]It is an explanatory view explaining the unit cell array of EEPROM.
[Drawing 9]It is a sectional view explaining NAND type EEPROM.
[Drawing 10]It is a circuit diagram explaining EEPROM.
[Description of Notations]
11 Memory cell array
17 Data comparison machine
19 Refresh control circuit
20 Variable voltage source

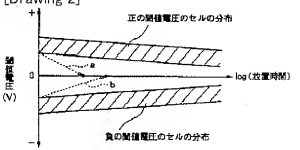
[Translation done.]

DRAWINGS

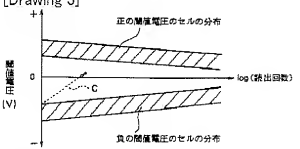
[Drawing 1]



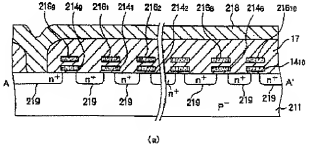
[Drawing 2]



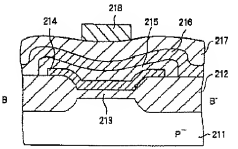
[Drawing 3]



[Drawing 9]

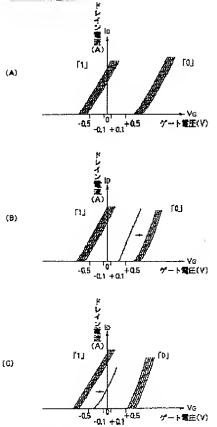


(a)

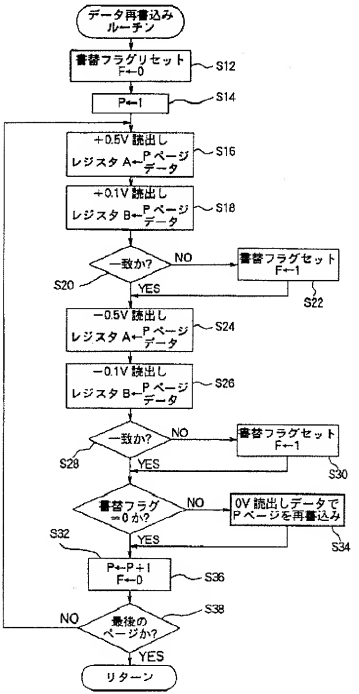


(b)

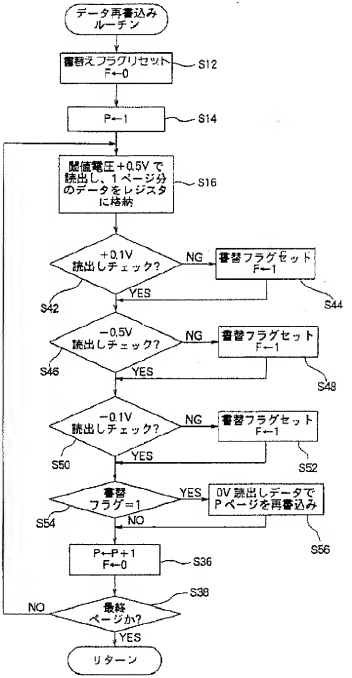
[Drawing 4]



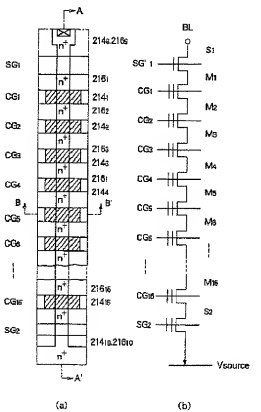
[Drawing 5]


データ再書込み
ルーチン
書替フラグリセット
F←0
S12
P←1
S14
+0.5V 読出し
レジスタ A←Pページ
データ
S16
+0.1V 読出し
レジスタ B←Pページ
データ
S18
一致か?
NO
書替フラグセット
F←1
S20
YES
S22
−0.5V 読出し
レジスタ A←Pページ
データ
S24
−0.1V 読出し
レジスタ B←Pページ
データ
S26
一致か?
NO
書替フラグセット
F←1
S28
YES
S30
書替フラグ
=0か?
NO
0V 読出しデータで
Pページを再書込み
S32
YES
S34
P←P+1
F←0
S36
S38
NO
最後の
ページか?
YES
リターン

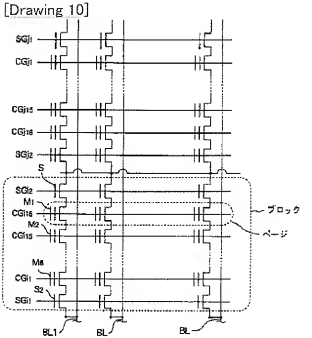
[Drawing 6]


データ再書込み
ルーチン
書替えフラグリセット
F←0
S12
P←1
S14
閾値電圧+0.5Vで
読出し、1ページ分
のデータをレジスタ
に格納
S16
+0.1V
読出しチェック?
NG
書替フラグセット
F←1
YES
S42
S44
−0.5V
読出しチェック?
NG
書替フラグセット
F←1
YES
S46
S48
−0.1V
読出しチェック?
NG
書替フラグセット
F←1
YES
S50
S52
書替
フラグ=1
YES
0V読出しデータで
Pページを再書込み
NO
S54
S56
P←P+1
F←0
S36
S38
最終
ページか?
NO
YES
リターン

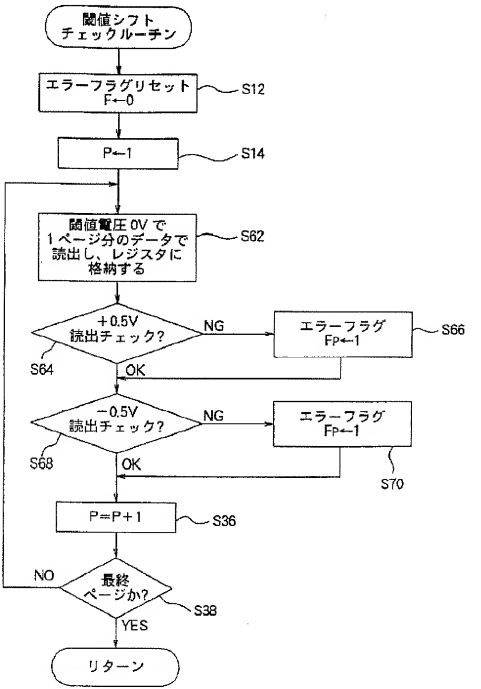
[Drawing 8]



[Drawing 10]



[Drawing 7]



[Translation done.]